## IN THE CLAIMS:

- (currently amended) A FIFO memory device comprising a storage stage and input stage, the storage stage comprising a plurality of <u>static</u>, non-volatile storage elements and the input stage comprising a plurality of <u>dynamic</u>, volatile storage elements.
- 2. (currently amended) [[A]] The FIFO memory device according to claim 1, wherein the storage stage comprises a static, non-volatile FIFO memory device.
- (currently amended) [[A]] The FIFO memory device according to claim 1, wherein the input stage comprises a <u>dynamic</u>, volatile FIFO memory device.
- (currently amended) [[A]] <u>The FIFO</u> memory device according to claim 1, wherein the
  memory device further comprises means for monitoring the status of the input stage
  and/or storage stage.
- 5. (currently amended) [[A]] The FIFO memory device according to claim 4 wherein the monitoring means includes a counter indicating the number of empty spaces.
- 6. (currently amended) [[A]] The FIFO memory device according to claim 1 wherein the input stage and storage stage are connected in series.
- 7. (previously presented) An integrated circuit comprising at least one memory device according to claim 1.

8. (new) A FIFO memory device comprising:

a storage stage and input stage, the storage stage comprising a plurality of nonvolatile storage elements and the input stage comprising a plurality of volatile storage elements; and,

a means for monitoring the status of the input stage and/or storage stage.

- (new) The FIFO memory device according to claim 8, wherein the storage stage comprises a non-volatile FIFO memory device.
- 10. (new) The FIFO memory device according to claim 8, wherein the input stage comprises a volatile FIFO memory device.
- 11. (new) The FIFO memory device according to claim 8 wherein the monitoring means includes a counter indicating the number of empty spaces.
- 12. (new) The FIFO memory device according to claim 8 wherein the input stage and storage stage are connected in series.
- 13. (new) An integrated circuit comprising at least one memory device according to claim 8.